Spread Spectrum Peak EMI Reduction Device

Description

P3P816711A generates a 1x LVCMOS low EMI Spread Spectrum clock of the input. The device accepts an AC or DC coupled external clock input at CLKIN. It reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

P3P816711A use the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

P3P816711A operates over a V_{DD} range of 3.3 V \pm 10% and is available in TSOP-6 package over a temperature range of 0°C to +70°C. P3I816711A operates over a temperature range of -40°C to +85°C.

Application

The P3P816711A is targeted towards EMI management in consumer electronics applications including Set Top Box.

Features

- 1x Low EMI Spread Spectrum Clock of the Input
- External Reference Input Clock: 30 MHz
- Output Clock: 30 MHz \pm 0.3%(typ)
- Low Inherent Cycle-to-Cycle Jitter
- Supply Voltage: $3.3 V \pm 10\%$
- LVCMOS Input and Output
- Available in TSOP-6 (6 Lead TSOT-23)
- Operating Temperature Range: -40°C to +85°C
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

http://onsemi.com





ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

P3P816711A



Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Туре	Description	
1	NC		No Connect	
2	GND	Power	Ground to entire chip.	
3	CLKIN	Input	xternal Reference Clock Input.	
4	NC		o Connect	
5	V _{DD}	Power	Power Supply to entire chip.	
6	ModOUT	Output	pread Spectrum Clock Output.	

Table 2. OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{DD}	Voltage on any pin with respect to V_{SS}		2.97	3.63	V
T _A	Operating Temperature	Commercial Industrial	0 -40	+70 +85	°C
CL	Load Capacitance			15	pF
C _{IN}	Input Capacitance			7	pF

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V _{DD} , V _{IN}	Voltage on any pin with respect to Ground	–0.5 to +4.6	V
T _{STG}	Storage Temperature	–65 to +125	°C
Ts	Max. Soldering Temperature (10 sec)	260	°C
TJ	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22-A114-B)	2.0	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Тур	Max	Unit
V _{DD}	Operating voltage		2.97	3.3	3.63	V
V _{IL}	Input low voltage		0		0.13xV _{DD}	V
V _{IH}	Input high voltage		0.85xV _{DD}		V _{DD}	V
V _{OL}	Output low voltage (ModOUT Output)	I _{OL} = 4 mA			0.4	V
V _{OH}	Output high voltage (ModOUT Output)	I _{OH} = -4 mA	2.4			V
I _{DD}	Dynamic supply current (Unloaded Output)				10	mA
I _{CC}	Static supply current (CLKIN pulled to GND)				0.5	mA

Table 5. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Тур	Max	Unit
f _{IN}	Input Clock frequency		30		MHz
f _{OUT}	ModOUT Clock frequency		30		MHz
t _{LH} (Notes 1, 2)	ModOUT Rise time (Measured from 20% to 80%)			5.0	ns
t _{HL} (Notes 1, 2)	ModOUT Fall time (Measured from 80% to 20%)			4.5	ns
T _{DCOUT} (Notes 1, 2)	Output Clock Duty Cycle (ModOUT) (Measured at 50%)	45	50	55	%
T _{JC} (Note 2)	Cycle-to-Cycle Jitter (ModOUT with Spread ON)		±200		ps
t _{ON}	PLL Lock Time (Stable power supply, valid input clock to valid clock on ModOUT)			3.0	ms

1. Parameters are specified with 15 pF loaded outputs.

2. Parameter is guaranteed by design and characterization. Not 100% tested in production.



Figure 2. Application Schematic

Table 6. ORDERING INFORMATION

Part Number	Marking	Temperature	Package Type	Shipping [†]
P3P816711A-06OR	BM1	0°C to +70°C	TSOP-6, Commerical (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE U







NOTES: DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

- 1. 2.
- CONTROLLING DIMENSION: MILLIMETERS. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM З.
- LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR Δ
- GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H. 5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS				
DIM	MIN	NOM	MAX		
Α	0.90	1.00	1.10		
A1	0.01	0.06	0.10		
b	0.25	0.38	0.50		
с	0.10	0.18	0.26		
D	2.90	3.00	3.10		
Е	2.50	2.75	3.00		
E1	1.30	1.50	1.70		
е	0.85	0.95	1.05		
Ĺ	0.20	0.40	0.60		
L2	0.25 BSC				
М	0°	-	10°		

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and

Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and 💷 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILIC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILIC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILIC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILIC obsent or any liability nor the rights of others. SCILIC products are not designed, intended, or authorized for use a components in systems intended for surgical implant into the body, or other applications are specified to the SCILIC of the S intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative